## REMARKS

Applicants appreciate the Examiner's thorough examination of the present application as evidenced by the final Office Action of October 11, 2002 (hereinafter "Final Action"). Applicants especially appreciate the indication that Claims 28 and 29 have been allowed and that Claims 5, 10, and 18 recite patentable subject matter. Applicants respectfully request the Examiner to take one final look at the rejected independent Claims 1, 12, 20, and 30 in light of the amendments and remarks presented herein. Applicants have amended Claims 20 - 22, 24 - 26, and 30 to numerically note the various references to "logic" used throughout these claims. Moreover, Applicants respectfully submit that the cited references, either alone or in combination, fail to disclose or suggest all of the recitations of independent Claims 1, 12, and 20.

Accordingly, Applicants respectfully request allowance of the present application and passing the application to issue. Alternatively, Applicants respectfully request entry of this amendment as introducing no new issues and narrowing the issues for further consideration.

**Independent Claims 20 and 30 Satisfy the Requirements of 35 U.S.C. §112**

Independent Claims 20 and 30 stand rejected under 35 U.S.C. §112, ¶2 as being indefinite. In response, Applicants have amended independent Claims 20 and 30 along with dependent Claims 21, 22, and 24 - 26 to numerically note the various references to "logic." Applicants, therefore, respectfully submit that Claims 20 - 22, 24 - 27, and 30 satisfy the requirements of 35 U.S.C. §112.

**Independent Claims 1, 12, and 20 are Patentable**

Independent Claims 1, 12, and 20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U. S. Patent No. 6,337, 999 to Orban (hereinafter "Orban") in view of U. S. Patent No. 5,293,401 to Serfaty (hereinafter "Serfaty"). Independent Claims 1, 12, and 20 are directed to demodulating a data signal transmitted from a digital source at a network sampling rate that is synchronized with a network clock. Claim 1, for example, is directed to a receiver that comprises a two-stage interpolator described as follows:

> ...the two-stage interpolator comprising:
>
> a polyphase interpolator, responsive to the digital samples of the data signal, that generates first and second estimates for each of the digital samples of the data signal; and
>
> a linear interpolator, responsive to the first and second estimates, that generates the interpolated digital samples...(Claims 12 and 20 include similar recitations).

According to the recitations of independent Claim 1, 12, and 20, the two-stage interpolator comprises both a polyphase interpolator and a linear interpolator. This aspect of the present invention is discussed in the Specification with reference to **FIG**. 7 at page 17, line 12 through page 18, line 21.

In rejecting Claims 1, 12, and 20 the Final Action cites col. 3, line 64, through col. 4, line 7 of Orban and states "FIR filter is polyphase and linear; if the filter was not linear, then the interpolation would not be linear; since the filter is linear and Orban does not mention quadratic interpolator or something similar, it is inherent for Orban's interpolator to be linear; also Orban mentions upsampling and this is inherently linear." (Final Action, paragraph 18). Applicants respectfully disagree with this interpretation of Orban's disclosure. Orban describes the filter **400** as a "half-band, polyphase symmetrical finite impulse response (FIR) filter (as is well-known in the art) to minimize the number of operations necessary to realize the filter while retaining phase linearity." (Orban, col. 3, line 67 - col. 4, line 1). Thus, the filter **400** described in Orban is a polyphase FIR filter. The combination of the upsampler **200** and the filter **400** shown in **FIG**. **2** of Orban may be considered a polyphase interpolator. None of the upsampler/filter combinations described in Orban, however, may be considered a linear interpolator as recited in independent Claims 1, 12, and 20.

The Final Action states "...Orban mentions upsampling and this is inherently linear." Orban explains at col. 3, line 65 - 66, however, that the upsampler **200** "inserts a zero between every sample." This operation is sometimes called "zero stuffing." Zero-stuffing may create a higher-rate signal whose spectrum is the same as the original signal over the original bandwidth, but has images of the original spectrum centered on multiples of the original sampling rate. Thus, zero-stuffing stands in sharp contrast to operations associated with linear interpolation in which lines are effectively drawn between neighboring samples

and the interpolated samples correspond to appropriate points along the lines between the samples.

Applicants submit, therefore, that neither Orban nor Serfaty contain any disclosure or suggestion of a two-stage interpolator that comprises both a polyphase interpolator and a linear interpolator as recited in independent Claims 1, 12, and 20.

For at least the foregoing reasons, Applicants respectfully submit that independent Claims 1, 12, and 20 are patentable over Orban in view of Serfaty, and that dependent Claims 2, 3, 5 - 11, 13, 14, 16 - 19, 21, 22, 24 - 27 are patentable at least by virtue of their depending from an allowable claim.

**Dependent Claim 5, 10, and 18 are Separately Patentable**

As mentioned above, the Final Action indicates that dependent Claims 5, 10, and 18 recite patentable subject matter. Therefore, Applicants respectfully submit that Claims 5, 10, and 18 are separately patentable.

## CONCLUSION

In light of the above amendments and remarks, Applicants respectfully submit that the above-entitled application is now in condition for allowance. Favorable reconsideration of this application, as amended, is respectfully requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (919) 854-1400.

It is not believed that an extension of time and/or additional fee(s), including fees for net addition of claims, are required, beyond those that may otherwise be provided for in documents accompanying this paper. In the event, however, that an extension of time is

necessary to allow consideration of this paper, such an extension is hereby petitioned under 37 C.F.R. §1.136(a). Any additional fees believed to be due in connection with this paper may be charged to IBM's Deposit Account No. 09-1990.

Respectfully submitted,

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**CERTIFICATE OF MAILING**

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Washington, DC 20231, on December 11, 2002.

Traci A. Brown
Date of Signature: December 11, 2002

**VERSION WITH MARKINGS TO SHOW CHANGES MADE**

**In the Claims:**

Please amend the following Claims by adding the language that is underlined ("__") and by deleting the language that is enclosed within brackets ("[ ]"):

20. (Twice Amended) A computer program product for demodulating, in a receiver, a data signal transmitted from a digital source at a network sampling rate that is synchronized with a network clock, comprising:

a computer readable storage medium having computer readable code means embodied therein, the computer readable code means comprising:

first logic configured to sample the data signal to produce digital samples at a first local sample rate that is synchronized with a local clock;

[first] second logic configured to interpolate the digital samples to produce first and second estimates for each of the digital samples, the [first] second logic configured to interpolate comprising:

third logic configured to use a polyphase interpolator to produce the first and second estimates;

[second] fourth logic configured to interpolate the first and second estimates to produce interpolated digital samples having a second local sample rate that is synchronized with the network clock, the second logic configured to interpolate comprising:

fifth logic configured to use a linear interpolator to produce the interpolated digital samples;

sixth logic configured to equalize the interpolated digital samples to produce equalized digital samples; and

seventh logic configured to decode the equalized digital samples to generate detected symbols therefrom.

21. (Amended) A computer program product as recited in Claim 20, wherein the sixth logic configured to equalize comprises:

eighth logic configured to use an adaptively fractionally spaced decision feedback equalizer that has tap spacing given by $pT/q$ where $T$ is a modulation interval associated with the network sampling rate and $p$ and $q$ are integers to produce the equalized digital samples.

22. (Amended) A computer program product as recited in Claim 20, further comprising:

eighth logic configured to maintain the synchronization between the second local sampling rate and the network clock via a sampling index signal.

24. (Amended) A computer program product as recited in Claim 20, wherein the receiver further includes an echo canceller coupling a transmitter to the receiver, further comprising:

eighth logic configured to receive at an input of the echo canceller transmit symbols from the transmitter that have a third local sample rate that is synchronized with the local clock; and

ninth logic configured to generate at an output of the echo canceller echo cancellation samples at the first local sample rate in synchronization with the local clock.

25. (Amended) A computer program product as recited in Claim 20, further comprising[;]:

eighth logic configured to identify a signaling alphabet, the seventh logic configured to decode being responsive to the logic configured to identify.

26. (Amended) A computer program product as recited in Claim 25, wherein the eighth logic configured to identify comprises:

ninth logic configured to establish a plurality of alphabet thresholds corresponding to valid data symbols;

tenth logic configured to compute an average value for the equalized digital samples corresponding to a particular alphabet threshold; and

eleventh logic configured to update the particular alphabet threshold with the average

value.

30. (Amended) A computer program product for demodulating, in a receiver, a data signal transmitted from a digital source at a network sampling rate that is synchronized with a network clock, comprising:

a computer readable storage medium having computer readable code means embodied therein, the computer readable code means comprising:

first logic configured to sample the data signal to produce digital samples at a first local sample rate that is synchronized with a local clock;

[first] second logic configured to interpolate the digital samples to produce first and second estimates for each of the digital samples;

[second] third logic configured to interpolate the first and second estimates to produce interpolated digital samples having a second local sample rate that is synchronized with the network clock;

fourth logic configured to equalize the interpolated digital samples to produce equalized digital samples;

fifth logic configured to decode the equalized digital samples to generate detected symbols therefrom;

sixth logic configured to identify a signaling alphabet, the fifth logic configured to decode being responsive to the logic configured to identify, the sixth logic configured to identify comprising:

seventh logic configured to establish a plurality of alphabet thresholds corresponding to valid data symbols;

eighth logic configured to compute an average value for the equalized digital samples corresponding to a particular alphabet threshold; and

ninth logic configured to update the particular alphabet threshold with the average value.